Ayoub Sadeghi

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EDUCATION

Master of Science (M.Sc.) in Electronic Engineering-Integrated Circuit Design, 2017-2019 Islamic Azad University of Shiraz, Shiraz, Iran

GPA: 17.12/20 (3.68/4)

Thesis Topic: "Designing New Exact and Approximate Comparators with Low Power Consumption and Delay Time for Image Processing Applications".

Thesis Grade: 17.99/20

Supervisor: Dr. Nabiollah Shiri

Selected Courses: Advanced Digital Electronics (18/20), Very Large Integration Circuit (VLSI) (19/20), Linear Integrated Circuits (17/20), Integrated Data Converters (19/20), Special Topics (FPGA Programing) (16/20), Bio-Electronic Circuits (20/20).

Bachelor of Science (B.Sc.) in Electrical Engineering-Electronics, 2012-2016
 Islamic Azad University - Fars Science and Research Branch (FSRIAU), Shiraz Iran
 GPA: 17.14/20 (3.47/4)

Selected Courses: Electronics (I, II, III), Electronic Lab. (I, II, III), Pulse Technique (Lab.), Telecommunication Circuits (Lab.), Filter & Synthesis of Circuit, Computer Architecture (Lab.), Microprocessors (Lab.), GPA for main courses: 3.7/4 (%85 of Courses with A+).

SKILLS

- Tools: HSPICE (Professional), MATLAB, Cadence Virtuoso (Professional), Xilinx ISE Design Suite (Intermediate), Proteus, Orcad Pspice, Electric-VLSI, COMSOL Multiphysics, Advanced Design System (ADS), GraphPad, Visio.
- > Hardware Languages: Verilog, VHDL.
- **Language:** Persian (Native), English (Fluent).

HONORS AND AWARDS

- Ranked among top 10% students of Electrical Engineering (Last 4 semesters of B.Sc. 2014-2016).
- **Ranked** among top 5% students of Integrated Circuit Designer (2019)
- Ranked first student and selected as research assistant in <u>Bioelectronics Integrated</u> <u>Circuits Lab</u> (2017-2019)
- Awarded student scholarship for tuition discount for 4 semester (Last 4 semesters of B.Sc. 2014-2016)

- > Awarded student scholarship for publishing scientific papers (2020-Current).
- Member of <u>Iran's National Elites Foundation</u> (November 2020).

RESEARCH INTERESTS

- Digital System Design.
- Embedded System Design.
- Reconfigurable Computing
- Computer Arithmetic and architecture
- Digital Arithmetic Circuits.
- > Approximate Computing.
- ▶ Reversible Logic and Quantum Systems.
- > Low Power and reliable Digital Design for Image Processing.
- > Modeling, Design and Testing Compact Devices (Transistors and Systems).

RESEARCH IMPACT AND CITATIONS

- ✤ 10 publications: 7 Journals and 3 Conferences.
- ✤ 6 Submission in Peer-Reviewed Journals.
- Citations (<u>Google Scholar</u> Since 2016): 23

PUBLICATION

Peer-Reviewed Journals

- J1. Mahmood Rafiee, Farshad Pesaran, <u>Ayoub Sadeghi</u>, Nabiollah Shiri, "An efficient multiplier by pass transistor logic partial product and a modified hybrid full adder for image processing applications", *Microelectronics Journal*, 118, 2021, <u>https://doi.org/10.1016/j.mejo.2021.105287</u>.
- J2. Mahmood Rafiee, Nabiollah Shiri, <u>Ayoub Sadeghi</u>, "High-Performance 1-Bit Full Adder with Excellent Driving Capability for Multistage Structures". *IEEE Embedded Systems Letters, August* 2021, <u>doi: 10.1109/LES.2021.3108474</u>.
- J3. Mahmood Rafiee, Yaqhoub Sadeghi, Nabiollah Shiri, <u>Ayoub Sadeghi</u>, "An approximate CNTFET 4:2 compressor based on gate diffusion input and dynamic threshold". *Electronic Letter*, 57: 650-652, 2021, <u>https://doi.org/10.1049/ell2.12221</u>.
- J4. <u>Ayoub Sadeghi</u>, Nabiollah Shiri, Mahmood Rafiee, High-Efficient, "Ultra-Low-Power and High-Speed 4:2 Compressor with a New Full Adder Cell for Bioelectronics Applications". *Circuits, Systems, and Signal Processing, 39, 6247–6275, 2020, <u>https://doi.org/10.1007/s00034-020-01459-x</u>.*

- J5. <u>Ayoub Sadeghi</u>, Nabiollah Shiri, Mahmood Rafiee, Parisa Rahimi, "A low-power pseudo-dynamic full adder cell for image addition". *Computers & Electrical Engineering, Volume 87, 2020,* <u>https://doi.org/10.1016/j.compeleceng.2020.106787</u>.
- J6. Ebrahim Abiri, Abdolreza Darabi, Mohammad Reza Salehi, <u>Ayoub Sadeghi</u>, "Optimized Gate Diffusion Input Method-Based Reversible Magnitude Arithmetic Unit Using Non-dominated Sorting Genetic Algorithm II". *Circuits, Systems, and Signal Processing*, 39, 4516–4551, 2020, <u>https://doi.org/10.1007/s00034-020-01382-1</u>.
- J7. Ebrahim Abiri, Abdolreza Darabi, <u>Ayoub Sadeghi</u>, "Gate-diffusion input (GDI) method for designing energy-efficient circuits in analogue voltage-mode fuzzy and QCA systems", *Microelectronics Journal, Volume 87, Pages 81-100, 2019,* <u>https://doi.org/10.1016/j.mejo.2019.04.001.</u>

✤ Conference

- **C1.** <u>Ayoub Sadeghi</u>, Nabiollah Shiri, "An Ultra Efficient and Reliable TG-PTL Based Full Adder Cell". The 5th International Conference on the New Horizons in the Electrical Engineering, Computer and Mechanical. Tehran, Iran, May 2020.
- **C2.** <u>Ayoub Sadeghi</u>, Nabiollah Shiri, "Tolerance Binary Comparator with Ultra-Power Saving Capability Based on Transmission Gate (TG) Technique". *4th International Conference on Electrical Engineering, Computer Science and Information Technology, Hamadan, Iran, February 2020.*
- **C3.** <u>Ayoub Sadeghi</u>, Nabiollah Shiri, "Small Area GDI Based Single Bit Magnitude Comparator with Low Power and High Speed". *4th Conference on Electrical Engineering, Mechanical Engineering, Computer Science and Engineering, Delhi, India, January 2020.*

Submitted in Peer-Reviewed Journals

- **S1.** <u>Ayoub Sadeghi</u>, Nabiollah Shiri, Mahmood Rafiee, Abdolreza Darabi, Ebrahim Abiri, "Voltage Over-Scaling CNT-Based 8-Bit Multiplier by Low-Threshold GDI-Based Counters". *Integration the VLSI Journal, Sep. 2021.*
- S2. <u>Ayoub Sadeghi</u>, Mahmood Rafiee, Nabiollah Shiri, Mahsa Tahghigh, "An efficient counter-based Wallace-tree multiplier with hybrid full adder core for image blending". *Frontiers of Information Technology & Electronic Engineering, Sep. 2021 (Minor Revision).*
- **S3.** Mahmood Rafiee, Nabiollah Shiri, <u>Ayoub Sadeghi</u>, Abdolreza Darabi, Ebrahim Abiri, "Low-Power and Fast-Swing-Restoration GDI-Based Magnitude Comparator for Digital Images Processing" *Circuits, Systems, and Signal Processing (Minor Revision).*

- **S4.** Nabiollah Shiri, <u>Ayoub Sadeghi</u>, Mahmood Rafiee, "High-Efficient and Error-Resilient GDI-Based Approximate Full Adders for Complex Multistage Rapid Structures". *Computers & Electrical Engineering, May 2021.*
- **S5.** <u>Ayoub Sadeghi</u>, Nabiollah Shiri, Mahmood Rafiee, Rahim Ghayour, "Tolerant and Low Power Subtractor with 4:2 Compressor and a New TG-PTL-Float Full Adder Cell". *Microelectronics Journal, 2021.*
- **S6.** Nabiollah Shiri, <u>Ayoub Sadeghi</u>, Mahmood Rafiee, Maryam Bigonah, "SR-GDI CNTFET-Based Magnitude Comparator for New Generation Programmable Integrated Circuits". *International Journal of Circuit Theory and Applications, August 2021 (Minor Revision).*

CURRENT PROJECTS

- Design and Synthesis of Approximate Floating-Point Arithmetic Circuits (HSPICE, MATLAB, Xilinx ISE) (August-Current)
 - Design and investigations of approximate floating-point circuits.
 - Practical image processing applications such as bio-image.

Compact Model of Virtual Source for CNTFETs for High-Efficient Digital Circuit Applications (HSPICE, COMSOL, MATLAB) (July-Current)

- Characteristic extraction of existed Models.
- Optimization of critical parameters proceeding using NSGA-II.
- Reliability test, and analysis of models in arithmetic applications.

TEACHING AND RESEARCH EXPERIENCE

- Teaching Assistant, CMOS VLSI course based on the book `CMOS VLSI Design A Circuits and Systems Perspective` for graduate students for two semesters. Islamic Azad University of Shiraz, under supervision of Dr. Shiri.
 (2019-2020)
- Teaching Assistant, Digital Circuit Design, based on the book `*Analysis and Design of Digital Integrated Circuits*` for graduate students for <u>three semesters</u>. Islamic Azad University of Shiraz, under supervision of Dr. Shiri.
- Teaching Assistant (Advanced Digital Electronics, Very Large Integration Circuit (VLSI), HSPICE & Cadence Virtuoso instructor), Islamic Azad University of Shiraz, under supervision of Dr. Shiri.
 (2017-Current)

 Research Assistant (Collaborated in Bioelectronics Integrated Circuits Lab with 12 members of Ph.D. and M.Sc. students), under supervision of Dr. Shiri.
 (2017-Current)

ACADEMIC EXPERIENCE

- Mentoring 10 graduate students in the way of completing their thesis, inspiring them with the research, including design and simulations of digital arithmetic circuits, writing the manuscript of the paper and thesis, attaining skills in research-related topics by analyzing and selecting up-to-date high quality articles, under supervision of Dr. Nabiollah Shiri. (2017-2019)
- Monitoring 4 PhD students with concentration on approximate computing dissertation and engage them with various challenges such as selection of the best research method, simulation methods, design and implementation at the layout level of integrated circuits, under supervision of Dr. Nabiollah Shiri. (2017-2019)
- Professional and scientific reviewer for articles written by graduate and Ph.D. students regarding technical challenges and writing edition, under supervision of Dr. Nabiollah Shiri. (2017-Current)
- English translator for technical papers for graduate and Ph.D. students,
 (2017-Current)
- Reviewer of an International conference. The 11th International Conference on Electronics, Communications and Networks (CECNet 2021) Beijing, China.
- Helping in Reviewing papers assigned to professors.

LANGUAGE SKILLS

- IELTS: Overall Score 6 (Listening: 6.0, Reading: 6.5, Writing: 5.5, Speaking: 6.5), expired, Feb. 2017,
 Will be retaken in Nov. 2021.
- ♦ GRE: Will be taken in Nov. 2021.

REFERENCES

- <u>Dr. Nabiollah Shiri</u> (Assistant Professor), Department of Electrical and Electronic Engineering, Islamic Azad University of Shiraz, Iran. *Email: <u>nabi.shiri@gmail.com</u>*.
- <u>Dr. Rahim Ghayour</u> (Full Professor), Department of Electrical and Electronic Engineering, Islamic Azad University of Shiraz, Iran. *Email: <u>rghayour@shirazu.ac.ir</u>*.
- <u>Dr. Ebrahim Abiri</u> (Full Professor), Department of Electrical and Electronics Engineering, Shiraz University of Technology, Shiraz, Iran. *Email: <u>abiri@sutech.ac.ir</u>*.